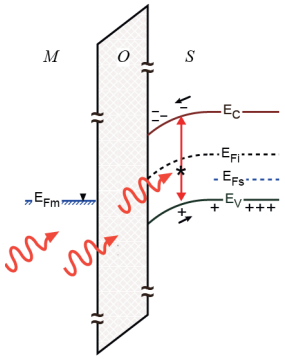
20 - Imaging **Name:**_____

In-Class Problems

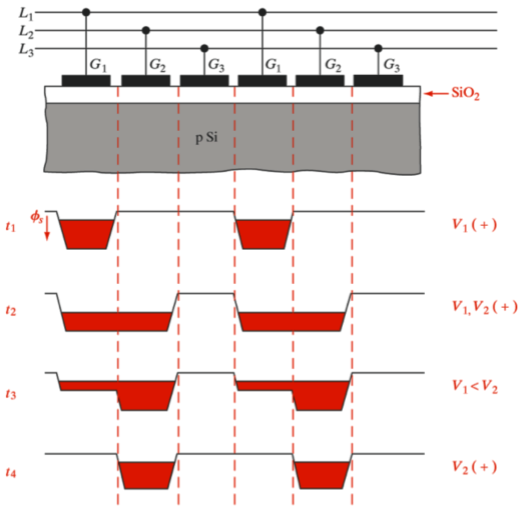
This is it! Last in-class HW session!

(1) Lets start out with a CCD imaging device, which is a good refresher for MOSFETs since the charge collecting well (a.k.a. the 'bucket') for a CCD pixel is just a MOS capactor. We will go back into topics from way earlier in the course in order to do this (a nice wrap-up problem!).

(a) Draw a simple band-diagram for an ideal MOS capacitor in a CCD imager with positive voltage applied to the gate (such that it creates a 'bucket' to capture photo generated electrons). Assume the substrate is p-type. Note, your 'metal gate' is likely something like ITO (discussed last lecture) which is a wide-bandgap and therefore transparent semiconductor. For simplicity, assume an ideal MOS capacitor. *Hint: see slide 7 in the lecture.*



(b) Next draw another diagram that shows how you will use positive voltage across multiple gates to moves charge to the edge of the array where it can be recorded by electronics. *Hint: see slide 9 in the lecture.*



(c) Next let's deal with how much light is hitting the semiconductor. Assume that on average we irradiate the device with $2x10^{12}$ photons/cm^2 every second, and that nearly all of that visible-spectrum light is absorbed in the first 2 μm of semiconductor beneath the oxide (*I got this from slide 14 lecture 15)*. That is about 0.7 μW/cm^2 (*not needed for your calculation, is just so you have some frame of reference, see slide 11 of week 15 for how to calculate).* First, calculate the optically generated excess carrier concentration assuming that carrier lifetimes due to recombination are $\tau_n \sim \tau_p = 10$ μs. *Hint, use this equation from slide 12 week 15, which tells you how recombination and optical generation balance out. You will need to convert the above info to g_{op} (1/cc-s) which is actually quite easy if you think about it. Make sure you keep units consistent!*

$$\delta_n = \delta_p = g_{op}\tau_n = g_{op}\tau_p$$

g_{op} = $2x10^{12}$ photons/cm^2 / 2E-4 cm = 10^{16}/cc-s

Excess = g_{op} * tau = 10^{16}/cc-s * 1E-5 s = 10^{11}/cc.

(d) Assume the substrate is doped to 10^{15}/cc with Boron. Question: how does that compare to your result from (c) in two ways: first, how big of a change (in terms of general orders of magnitude) is the concentration for electrons, and second is the change in holes below the doped level? (which is important, because you need dopings for semiconductor devices to work, and if the optical or thermally generated carriers are even more than the doped levels, then your device is likely in trouble).

$n_p = n_i^2/N_A$ = 2.25E20 / 1E15 = 2.25E5/cc

So…. the optically generated electron concentration is SIX orders of magnitude greater than this thermally generated concentration of electrons (which is good!).

So…. the optically generated charge is FOUR orders of magnitude less than the doped hole concentration (which is also good!).

(e) So hopefully in (d) you showed that you are setup for success: a large change in the minority carrier concentration due to light, and you are not overwhelming your doped majority carriers. Next, calculate the maximum depletion width that can be achieved and calculate the diffusion length for electrons in this material. *Hint: use this equation found on slide 23 in the lecture for week 12.*

$$W_m = 2\sqrt{\frac{\varepsilon_s kT\ln(N_a/n_i)}{q^2 N_a}}$$ = 0.87 μm.

Remember, diffusion length is just the square root of diffusion coefficient times lifetime. Assume for this doping level electron mobility is ~1000 cm/s/(V/cm). And you can use this equation from lecture 2.

$$D_n = \mu_n kT/q$$ = 1000 * 0.0259 = 25.9 cm^2/s

$L_n = (D_n \tau_{au_n})^{1/2} = (25.9*1E\text{-}5)^{1/2}$ = 160 μm.

As you complete this calculation, you will notice that W+Ln is much longer than the depth of photon absorption stated in part (a), and therefore when you go onto the next part you should replace (Ln+Wm) instead with just the 2 μm which was stated in part (a). This may not always be the case (e.g. higher doping levels which shorten Ln and Wm and longer wavelengths of light which have weaker absorption in Si).

(f) Whew, almost there. Next…. assume the pixel area is 100 μm x100 μm (these are the horizontal dimensions of the 'bucket'). Calculate the optical generated current if light were continually shining on this 'bucket' beneath the MOS capacitor. *Hint: use this equation from slide 9 in the lecture and do the substitution mentioned above! Remember, careful with units!*

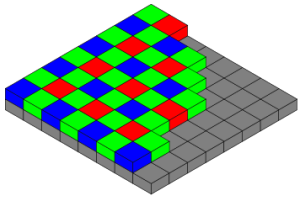
$I_{op} = qg_{op}A\left(L_n + W_{\max}\right)$ = 1.6E-19 * 10^{16} *0.01x0.01* 2E-4 = 32 pA. Cool stuff!

(g) Finally… figure out the amount of charge you will collect in this bucket per frame if we have a frame rate of 60 Hz. *Equation below is also from slide 9.* This is how much charge some sort of amplifier at the edge of the CCD will receive in order to read the pixel. *With 'some electronics', if you wanted, you could design the rest of what is needed to make the CCD work.*

$Q_{op} = I_{op} \times t_f(s)$ = 32E-12/60 = 0.533 pC.

The answer might seem small, but if your CCD had 1000x1000 pixels (1 million pixels), then at MINIMUM *it would need to read out this charge per pixel in 1 µs or faster. That leads to a decently large current (charge/time). In practice, the read out will have to be much faster than that, because the CCD spends most of its time just sitting there collecting light in its 'buckets', then doing a super-fast movement of all the buckets to the read out electronics, then repeating that process.*

(2) Now let's switch gears to CMOS imaging arrays. CMOS imaging arrays are faster because they have at least one CMOS transistor at each pixel and therefore can be addressed using row-column addressing (less of a serial scanning process). This also means you can get to higher pixel densities. They also require less power. And, they can be made using CMOS fabrication lines: lots of existing manufacturing infrastructure and tools, which reduces their cost. This lower cost, is their biggest advantage commercially. Now….



(a) As shown in the image at right, they use monochrome Si CMOS pixels that are covered with RGB color filters, but there are twice as many green filters as red or blue. Why? *Hint, we covered this in today's lecture 20, or you can remember the LEDs lecture and lm/W (brightness) for colors as they are perceived by the human eye.*

The human eye is much more sensitive to green light than red or blue, and the imaging array therefore has to mimic the human eye if it is going to properly interpret overall brightness.

(b) Here is a commercial CMOS chip.

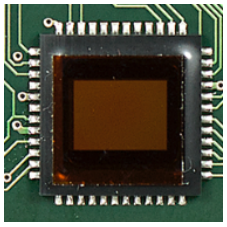
Aptina IMAGING

MT9P031: 1/2.5-Inch 5Mp Digital Image Sensor
Features

1/2.5-Inch 5Mp CMOS Digital Image Sensor

MT9P031 Data Sheet, Rev. G

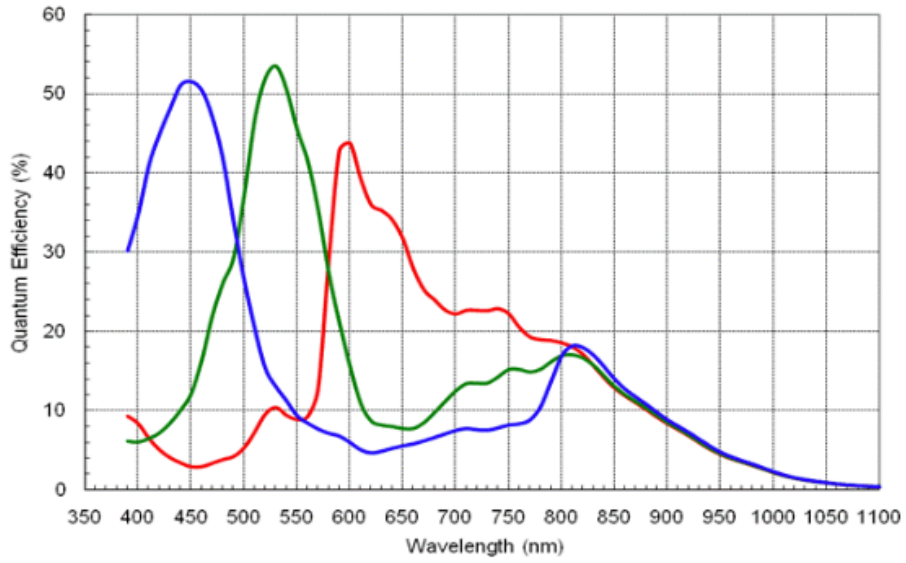
For the latest data sheet, refer to Aptina's Web site: www.aptina.com

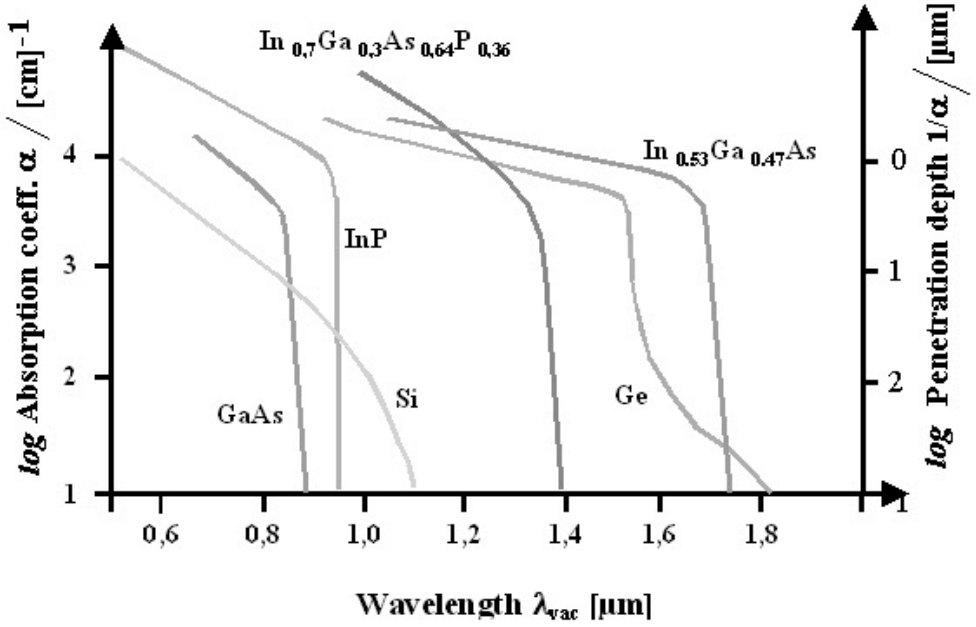


Notice the 1st plot below from the spec sheet for this chip, which is quantum efficiency vs. wavelength. Quantum efficiency for a photodiode or an imaging array = (# electrons collected / # photons in). The color filter effect on quantum efficiency is easy to see and obvious (if a color filter absorbs light outside of the desired wavelength range, that absorbed light is absorbed in the color filter material where it does NOT generates electrons.

Question: notice how the quantum efficiency generally decreases as you get closer to the bandgap energy of Si (Eg= 1.12 eV= 1240 / 1107 nm). Why is this? Hint, see the second plot below which is from lecture 16 on photodiodes.

Simple, at some point the light is so weakly absorbed that most of it passes *through* the region where it needs to be absorbed (is absorbed deeper in the Si wafer, where there is no PN junciton to collect the charge).





(3) Some old-timey review from lecture 1 :)

(a) Check below, how a thermally generated electron-hole pair allows electrical conduction.

__ (a) the hole is positive charge due to lack of an electron, and Si atoms can trade back and forth this lack of an electron.

__ (b) the electron is freed from the Si atoms and can freely move in between Si atoms.

__ (c) neither of the above.

__ (d) both of the above.

d

(b) An insulator like SiO_2 or Al_2O_3 has no electrical conduction, why is this typically?

__ (a) it has no conduction band or valance band.

__ (b) it has a conduction and a valence band, but so far apart in energy that at 300K no electrons/holes are generated.

__ (c) neither of the above.

b

(c) Most often Si is used with n or p-type doping, if we add As to Si, it will bond like other Si atoms and:

__ (a) it has one less electron than Si so it will create an electron (n-type).

__ (b) it has one more electron than Si so it will create an electron (n-type).

__ (c) it has one less electron than Si so it will create a hole (p-type).

__ (d) it has one more electron than Si so it will create a hole (p-type).

b

(d) Si is doped with B atoms, the B atoms have one less electron with Si, so when they bond with the Si they 'steal' and electron from the Si which creates a hole, and which cause B to have negative charge. Which is true:

__ (a) the positively charged holes created by B atoms add to the total electrical conductivity of the Si.

__ (b) the now negatively charged B atoms add to the total electrical conductivity of the Si.

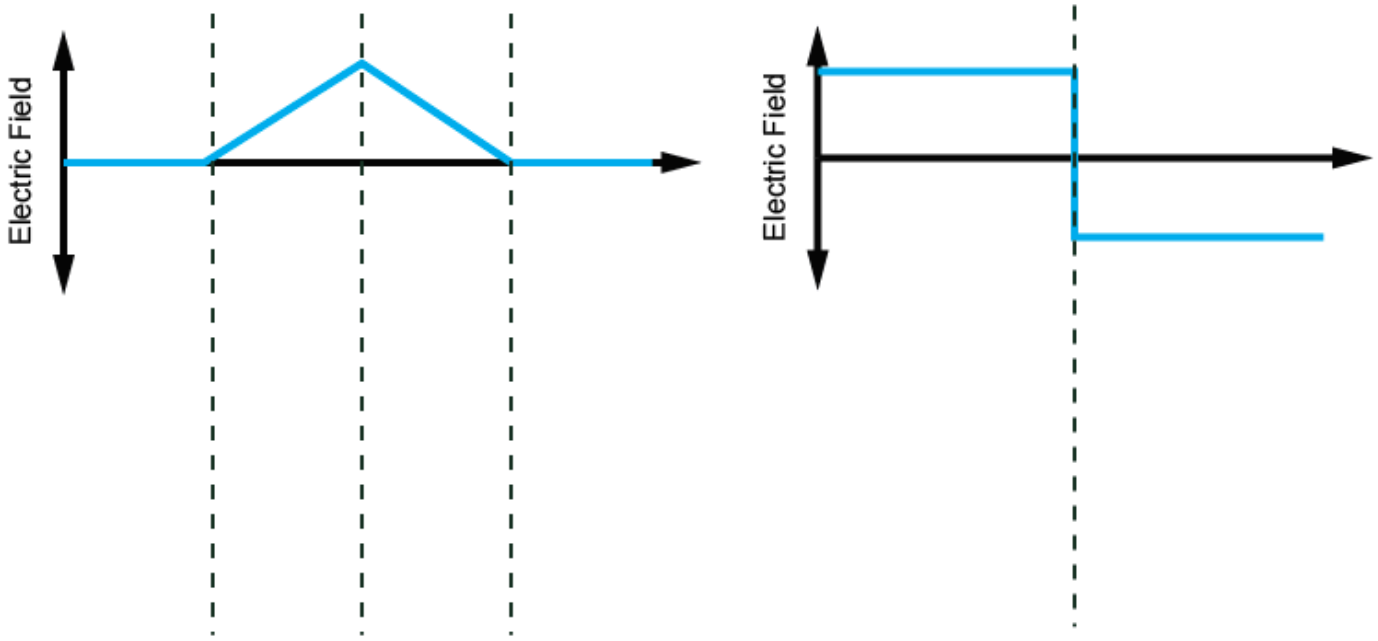
__ (c) both of the above.

__ (d) neither of the above.

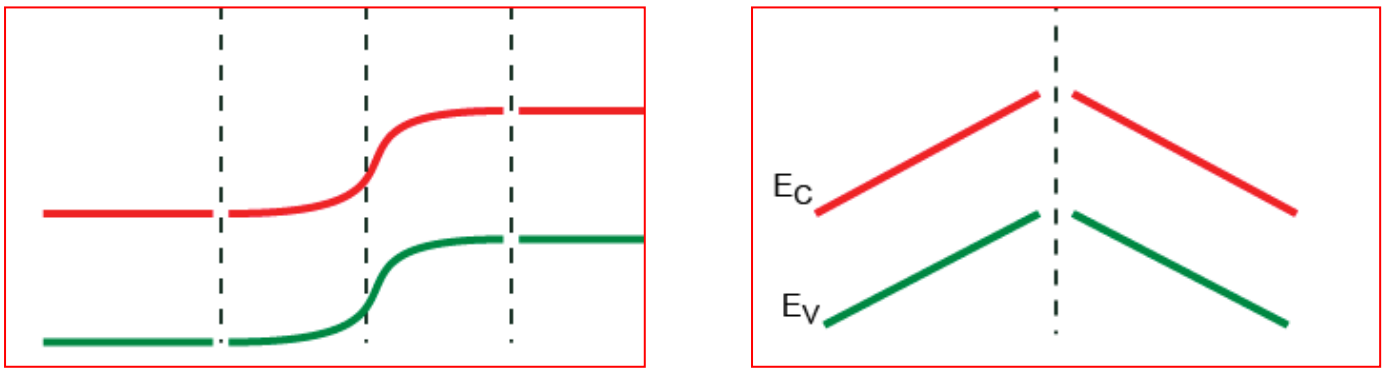
a

(4) Some more old-timey review from lecture 3 :)
E-field causes band diagrams to have slope! Anytime you have E-field, you know it means the bands must bend! Redraw each of these E-field plots on the board, and below the E-field plots draw the corresponding band diagrams (don't worry about the Ef or dopings, just plot the conduction and valence bands).

To help solve this problem, use the electrons=water and holes=bubbles analogy and think how they each should move (left or right) in the E-field. Assume the E-field is measured in the direction from left to right. Remember, higher E-field should make the bands slope steeper! (postive E-field = positive bands slope / negative E-field = negative bands slope).



Answer:



(5) And… last bit of old-timey review from lecture 7 :)

(a) See the spec sheet I-V curves below. Why is I_C exponential vs. V_{BE}? The answer is simple.

Because it is a diode being turned on in forward bias, right?!

(b) See the spec sheet I-V curves below. For Ic vs. Vce, what is the amplification factor (Beta)? To be sure, pick 2 or 3 base-currents and collector currents to calculate Beta.

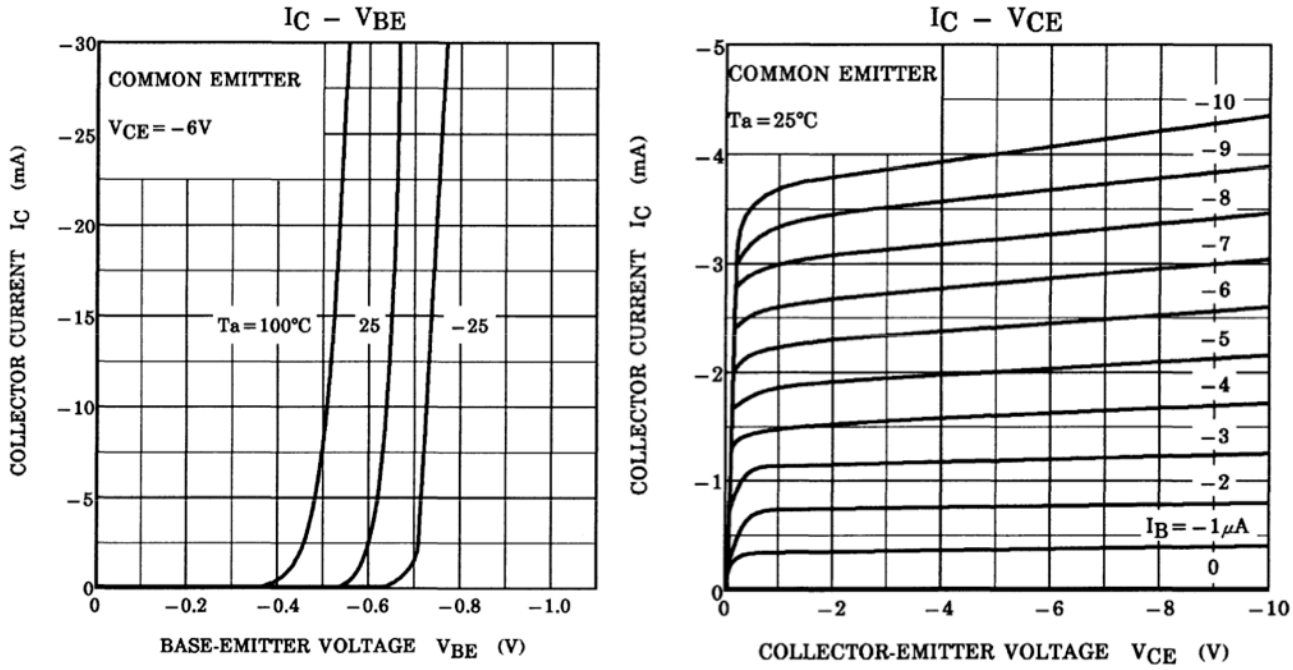
I'll measure at Vce = 4 V: 3.6 mA / 9 µA ~ 400 or so, 2 mA / 5 µA ~ 400 or so…

(c) See the spec sheet I-V curves below. As Vce is increased it takes a little bit (looks like ~0.5V) to get the BJT amplification going. Question: basically all the Vce voltage drop occurs where in the BJT? … and why is the collector current fairly constant as V_{CE} is further increased?

All Vce is applied across the base-collector. The base-collector is reverse biased, and reverse bias current is DRIFT and independent of voltage (so Ic is fairly constant with Vce).

(d) Based on your answer to (f), that increasing Vce should increase the base-collector depletion region, right? An increasing depletion region should cut into the base and reduce Wb (the un-depleted width of the n-type base). So, if increasing Vce reduces Wb a bit, then why the slight positive slope for Ic vs. Vce?

Increase Vce → Increase Vbc → Increase depletion width for bc (Wbc) → Reduce Wb → and a smaller Wb causes less holes to recombine w/ electrons in the base, which gives a larger Ic/Ib or a larger beta (amplification factor). So, the positive slope you see is the amplification factor increasing as you increase Vce!



(6) And… very last: https://www.youtube.com/watch?v=b9434BoGkNQ